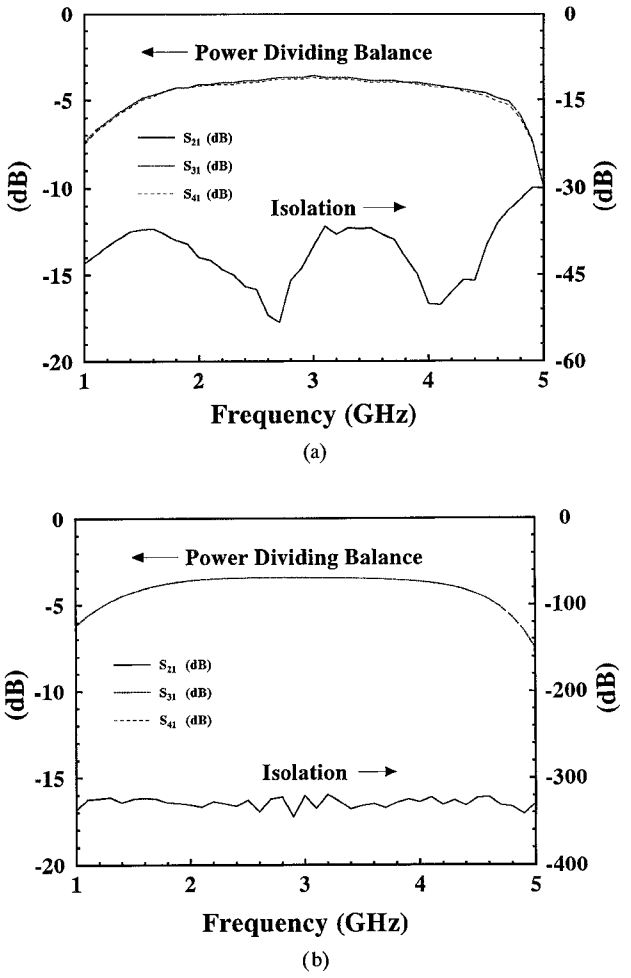

Fig. 6. Insertion loss of a slotline cross-over hybrid ring coupler; (a) measured results and (b) calculated results.

ACKNOWLEDGMENT

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A Low Noise, Phase Linear Distributed Coplanar Waveguide Amplifier

K. Minot, B. Nelson, and W. Jones

Abstract— **Details of the design, fabrication, and measured data for an InGaAs high electron mobility transistor (HEMT) decade-bandwidth distributed coplanar waveguide (CPW) amplifier are presented. Comparison to a similar microstrip design is made. The design methodology highlights described here include CPW transmission line loss modeling. The circuit features the best reported CPW distributed amplifier noise figure and phase performance over 2–20 GHz as well as an on-chip bias network and low dc power consumption. The minimum measured noise figure is 2.1 dB with 11 dB maximum gain. The measured phase linearity is less than ±5° over 2–20 GHz which makes this circuit well suited for system phased array applications where phase matching and linearity are a primary concern.**

I. INTRODUCTION

Advances in space and ground communication technologies are pushing the limits of such system requirements as size, weight, and performance. There is a constant desire to produce the smallest, lightest unit with the most outstanding performance yet seen over a broad bandwidth of frequencies. Phase linearity and chip to chip phase matching are becoming increasingly more critical system performance characteristics. As a result, the distributed amplifier (DA) has become an ideal topology choice for subsystem phased array elements requiring signal amplification [1]–[3]. Not only does the distributed topology offer typically greater than octave bandwidth performance, but it also offers excellent phase linearity due to the transmission line characteristics inherent in its topology. A DA is made up of a set of cascaded devices, which act as shunt capacitance, connected together by high impedance transmission lines that simulate inductance. A distributed transmission line constructed as such will have a near constant group delay and, hence, low phase deviation from linear below the cutoff frequency of the artificial transmission line.

In addition to the phase linear properties of the DA structure, we present a design for which simplified processing and system use are also advantages. This CPW design requires no vias or backside gold processing during wafer fabrication since the ground plane is entirely on the top surface of the circuit. Thus, all ground connections can be made from the top of the circuit when used in higher level system integration. This paper will describe CPW transmission line modeling, circuit design, fabrication, and performance of a 2–20 GHz CPW DA.

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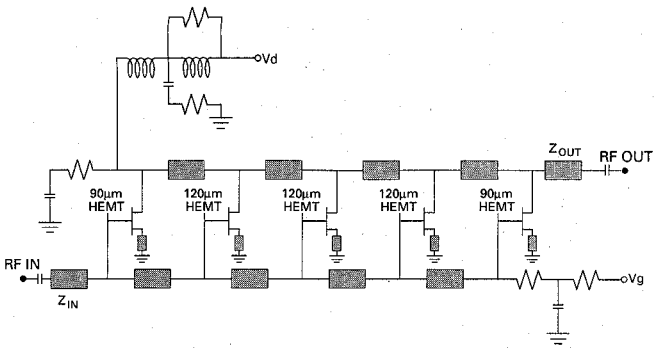

Fig. 1. Circuit schematic of the 2–20 GHz CPW DA.

II. Design

The coplanar waveguide distributed amplifier (CPW DA) design was based on an existing 5-section standard microstrip DA [3]. Both DA's were fabricated using 0.2 μm T-gate length high electron mobility transistors (HEMT's) on InGaAs material. The combination of material growth and T-gate topology provides superior transconductance (500 mS/mm), high cutoff frequency ($f_t > 60$ GHz), and inherently low noise figure well suited for broadband requirements ($NF_{\min} = 0.5$ dB at 12 GHz).

Similar to the reported DA [3] that was designed in microstrip, this CPW DA uses five cascaded cells (Fig. 1). The input and output cells each use a 90 μm gate periphery HEMT. The three middle cells each use a 120 μm gate periphery device for a total gate periphery of 540 μm.

The circuit was designed for use with 50 Ω source and termination impedances. The input and output signal ports used the ground–signal–ground structure common to CPW circuits. The dimensions of the CPW center conductor and gap between ground planes were chosen for 50 Ω impedance. MIM capacitors were used at the RF input and output of the chip as dc blocks. The dimensions of these capacitors were selected to match those of the center conductor such that step discontinuities could be minimized.

Initial CPW transmission line dimensions were chosen to match the impedances of the equivalent transmission lines from the microstrip version. The gate and drain CPW lines connecting the five devices were constrained so that a uniform ground to ground spacing could be maintained throughout all five cells to enable a simplified circuit layout. The gap and center conductor widths were allowed to vary as the required impedance varied and were tuned for optimal performance.

Another design concern was the maintenance of CPW ground continuity throughout the circuit. This was accomplished by using airbridge connections between the ground planes on either side of the RF signal lines, especially where the signal lines were long. Airbridge jumpers were used in at least one location for each gate and drain loop between devices as shown in Fig. 2. Additional jumpers were used across the gate and drain dc bias lines as well. The on-chip high impedance dc bias network was converted from the original microstrip version to a CPW implementation. Measured CPW spiral inductor data was used in the design. To dampen the predicted series resonance of the inductors, a shunt resistor was provided across the larger inductor and a shunt resistor-capacitor was placed between the two inductors.

During the initial design phase, it was discovered that the microwave simulation software, LIBRA, assumed lossless CPW transmission lines. To compensate for this, a simple resistive loss was artificially introduced into the circuit simulation using resistors whose values were ideal resistors based on the physical characteristics of the lines. The calculation of the dc resistance ($R_{\rm dc}$) of a CPW

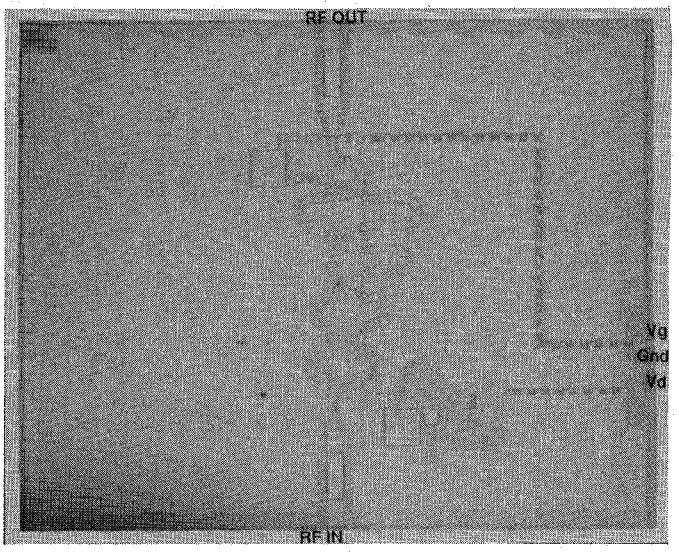

Fig. 2. Photograph of the 2–20 GHz CPW DA.

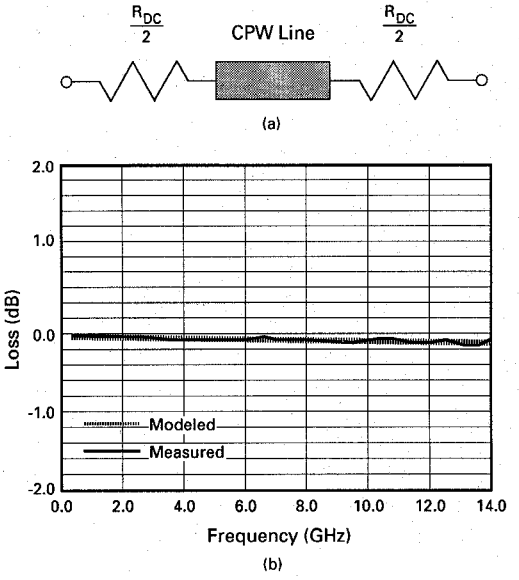

Fig. 3. Measured versus modeled performance of the simple lossy CPW transmission line.

transmission line was based on the cross-sectional area per unit length as in (1).

$$R_{\rm dc} = \frac{\rho l}{wt} \tag{4}$$

where $\rho = 1/\sigma$ is the resistivity of the top metal layer, w is the width of the CPW transmission line, t is the top metal thickness, and l is the CPW transmission line length, all in microns. Although dispersive frequency dependent loss mechanisms were not included in the CPW transmission line model, it was found that measured line loss below 20 GHz matched the model reasonably well. Fig. 3 shows the simple lossy CPW transmission line model and measured versus modeled performance.

Scaleable linear HEMT device models were developed from on-wafer RF S-parameter and noise parameter measurements of discrete devices to simulate small signal noise and S-parameter behavior. This model has been presented by Nelson *et al.* [4].

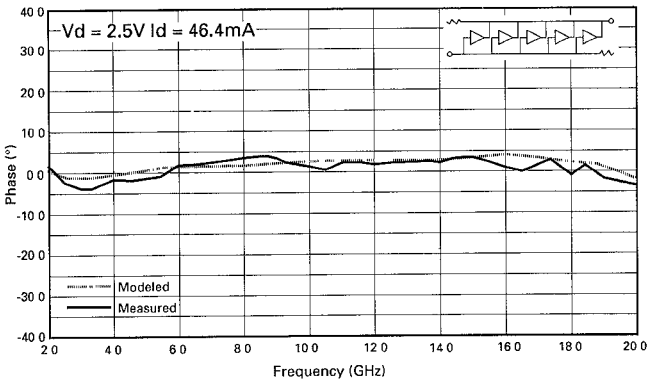

Fig. 4. Measured versus modeled phase linearity of the 2–20 GHz CPW DA.

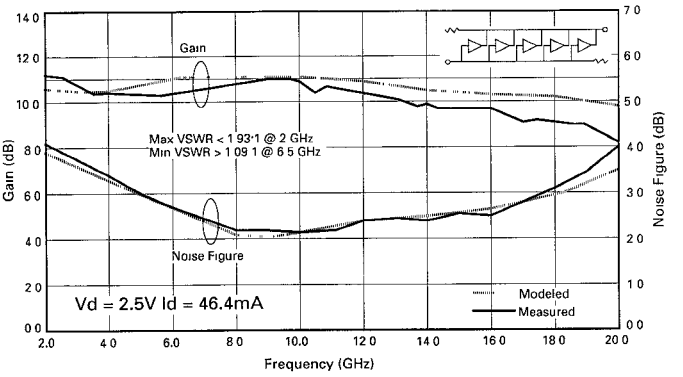

Fig. 5. Measured versus modeled gain and noise figure performance of the 2–20 GHz CPW DA.

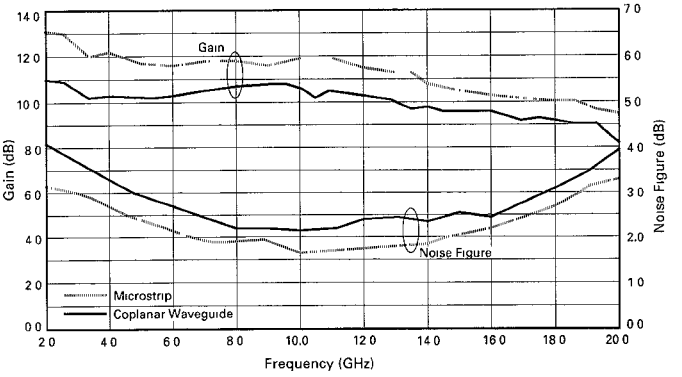

Fig. 6. Measured gain and noise figure performance of a CPW DA compared to a similar microstrip DA.

III. Fabrication

The circuit described here was fabricated by the TRW Electronic Systems Group GaAs Foundry. The HEMT MMIC process includes a multiple oxygen implant to isolate the active regions and a AuGe metallization for source-drain ohmic contact, which is rapid thermal alloyed to insure good ohmic contact to the Two-Dimensional Electron Gas Channel [5]. Other steps in the HEMT MMIC process include nichrome for circuit resistors, a low temperature SiO_2 layer (the current TRW process uses Si_3N_4) for MIM capacitors, first level interconnect metal and top metal to form transmission lines, top plates for capacitors and inductors. The 0.2 μm T-gate is formed using a Philips Electron Beam Lithography system to write the gate pattern in a PMMA/P(MMA-MAA) mixture [6]. The opening in the PMMA is used to recess the device current to a level that will ensure device pinchoff, optimum minimum noise figure, and maximum associated gain at a low power bias condition. An optional low temperature Si_3N_4 layer can be used to passivate the Ti/Pt/Au T-gates after liftoff. The MMIC's are completed by thinning the 3-inch wafer down to 4 mils (typical) and plating up to 3 μm of Au to interconnect the source grounds. Extensive in-process monitoring is practiced in order to ensure a reproducible, high yield process, with demonstrated low noise performance up to 60 GHz [7].

IV. Performance

S-parameters and noise figure were measured on-wafer using an RF test station and an ATN, Inc. noise parameter test set. A photograph of the 2–20 GHz CPW DA is presented in Fig. 2. A minimum 50 Ω noise figure of 2.1 dB was achieved with a maximum gain of 11 dB across the band of interest. Worst case VSWR was measured to be approximately 1.9:1 near the band edge. Phase linearity (deviation from linear after a constant 50 Ω delay line is removed) held within $\pm 5^\circ$ over the entire 2–20 GHz frequency range. Measured and modeled performance of phase, gain, and noise figure are shown in Figs. 4 and 5. Phase matching across the wafer was 4° peak to peak. Phase linearity for the microstrip DA was held within $\pm 7^\circ$ over the entire 2–20 GHz frequency range. A comparison of the measured performance of the CPW DA and the microstrip DA is presented in Fig. 6, where the data were taken from different wafers. The offset in the gain and noise between the two designs can be attributed to differences in transconductance from the different wafers. Simulated performance of the CPW and microstrip DA shows good correlation given the same transconductance. RF yields per wafer were typically 40% for both the CPW and microstrip circuits.

V. Conclusion

The 0.2 μm T-gate TRW InGaAs HEMT device was used in a distributed 5-cell CPW topology MMIC to produce a low noise, phase linear amplifier covering a decade bandwidth of frequencies. The CPW circuit offers simplified processing and lower cost over similar microstrip amplifiers, while maintaining phase linearity, low noise figure, and adequate gain.

Acknowledgment

The CPW DA and microstrip DA described here was processed at the TRW Electronic Systems Group GaAs Foundry. The authors would like to acknowledge D. C. Streit for MBE growth, P. Liu and A. Freudenthal for EBL T-gate support, L. Go, R. Topacio, and V. Zamora for MMIC fabrication, and C. Hur and F. Oshita for RF testing support. Other support was provided by various members of the Advanced Microelectronics Lab and RFPDL during the development of this work.

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Coplanar Waveguide Transitions to Slotline: Design and Microprobe Characterization

Wes Grammer and K. Sigfrid Yngvesson

***Abstract*—Three types of coplanar waveguide/slotline baluns, suitable for monolithic integrated circuits, are designed and characterized to 40 GHz, using microwave wafer probes. The results from each are compared, and methods of biasing the slotline discussed.**

I. Introduction

The use of coplanar waveguide has several distinct advantages over microstrip as a medium for monolithic microwave integrated circuits. Its uniplanar structure eliminates the need for ground vias, which introduce an undesirable parasitic inductance and limit the performance at high frequencies. Coplanar lines can also be scaled to smaller widths for a given impedance, without the need for substrate thinning. Lastly, integration of devices in series or shunt is simple. Integration with other uniplanar structures, such as tapered-slotline antennas [1] or slot rings [2]–[3], requires a suitable circuit transition from coplanar waveguide (CPW) to slotline.

Three different types of CPW–slotline transitions were identified in the literature. These are shown in Figs. 1–3, along with their approximate equivalent circuit models. The first, referred to here as Type I, is based on a CPW-slotline T-junction [4], [5]. A variation on this type uses a grounded substrate and finite-width strips for the slotline, exciting a coupled microstrip-like quasi-TEM mode [6]. The second (Type II) is a uniplanar realization of the compensated Marchand balun [7]–[9]. The third (Type III) is a CPW equivalent of the double-junction microstrip-slotline balun [10]. The elements Z_{1-6} in Fig. 3 refer to the input impedances of the stubs and transmission lines, as seen from the junction. All of these designs are uniplanar, but require one or more bond wires or air bridges at the junction for odd-mode suppression in the CPW.

The aim of this work was to investigate how the earlier designs could be translated to MMIC-type circuits (on high-resistivity silicon substrates), and toward higher frequencies, up to 40 GHz.

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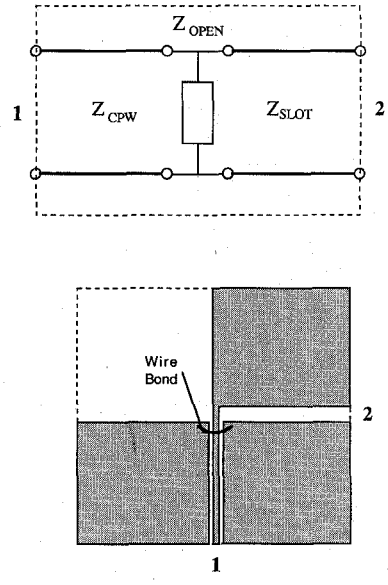
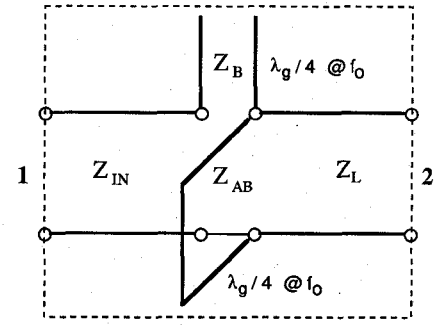


Fig. 1. Type I balun and equivalent circuit.



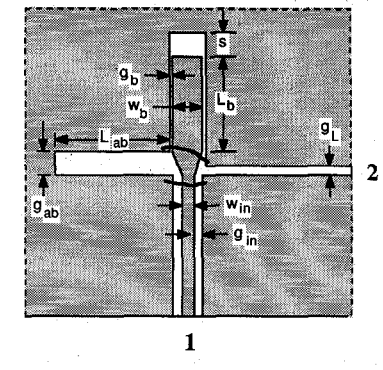


Fig. 2. Type II balun and equivalent circuit.

II. Analysis and Design

A. Type I Balun

Assuming the unterminated side of the T-junction to be a decent broadband open, the conductor gap and width dimensions of the transmission lines in Fig. 1 are chosen to give an approximate 50 Ω match. The CPW dimensions are made small to minimize parasitic effects at the junction. Using the transmission line analysis program PCAAMT [11], for a silicon substrate ($\epsilon_r = 11.9$) with a thickness $h = 0.33$ mm, a width and gap size of 25 μm was found to be